SVL Technique for Reduction of Power Consumption in CMOS Full Subtractor

[1]Bikshalu Kalagadda, [2]Madhavi Latha Pedada, [3]Keerti Kumar K
[1,2]Dept. of ECE, Kakatiya University, Warangal, India
[3]Dept. of ECE, National Institute of Technology Warangal, India

Abstract
In this paper a Self Controllable Voltage Level (SVL) Technique is used to design a Full Subtractor. The circuit supplies an increased dc voltage to the required active-load circuit and decreases the dc voltage supplied to the load circuit in standby mode. Full Subtractor consumes low power and low Leakage when compared to conservative design with SVL technique. The total power dissipation can be reduced by applying the upper Self Controllable voltage level (U-SVL) technology that uses increased supply potential and Lower Self Controllable voltage level (L-SVL) technology that uses raised ground potential. This paper represents how to manage power by means of SVL techniques. Based on power consumption, propagation delay, speed and layout area, the Full Subtractor using SVL technique is highly preferable as compared to conventional design. Low-power method is anticipated to reduce power in nanoscale CMOS-VLSI systems using SVL technique. The results illustrate that there is noteworthy reduction in Power incorporation of Full Subtractor in allusion mode. This design is greatly helpful in designing the systems that consume low power. The circuit is designed using Cadence Tools in 45nm Technology.

Keywords
SVL technique, Full Subtractor, U-SVL, L-SVL, CMOS Circuit, Low Power and High Speed.

I. Introduction

The Full Subtractor is a logical circuitry that represents the small unit for subtraction in digital systems. Most of the gates used in digital design are irreversible for consequence NAND, OR and E-XOR gates [1]. For this reason the reversible logic amalgamation of Full Subtractor is very decisive for designing of diminutive portable devices [2]. There are abundant prospective logic designs which can provide high-quality concert when compared to the basic CMOS logic design [3]. The performance inference of Full Subtractor is envisaged on the basis of area, delay and power consumption [4, 12]. To execute the designing, full traditional realization and replication of Subtractor at the CMOS circuit level suggests CMOS 45nm technology [5]. It is intended to check if the circuit may possibly execute with all the likely combinations of the input in addition to the logic performance [6] and to estimate the standard of the output signals in stipulations of voltage levels [7]. The admittance presentation of the circuit is in measured terms of speed, area, delay and power utilization [8, 15]. The Full Subtractor using CMOS circuit uses numerous completely divergent logic designs are conferred and combined into the integrated design methodology. The conservative Full Subtractor CMOS circuit diagram is shown in Figure 1 and its truth table shown in Table 1. The number of logic gates required to compose this Subtractor are added so as to augment the number of CMOS circuits. Consequently the delay and area will be huge. The obligation for optimizing Full Subtractor using cadence is to reduce the area, delay and power consumption [10-11]. The CMOS gpdk 45nm technology include the cadence representation Editor and Analog Environment software used to produce a schematic diagram and realization of our simulation. Conversely, it contains the Cadence Virtuoso Editor that permits us to propose the layout of the Full Subtractor, as well as to evaluate the performance of many concert parameters for the circuit. In addition, transitory analysis is achieved [17]. The design of a Full Subtractor is selected in such a way that the area is reduced as much as possible. The circuit is used for arithmetic calculation in the processor and for calculating address. A Stack pointer is used for subtraction in push-pop logical operation to store the address. The simplest combinational circuit that performs the arithmetic subtraction operation of 2- binary digits is called Full-Subtractor [18]. Static and dynamic power dissipation are the two major factors that affects the Power dissipation in any Full Subtractor circuit . The static power dissipated is the manifold of supply voltage and leakage current. The leakage current is expressed as

$$I = I_{os}\left(e^{qvkT} - 1\right) \quad (1)$$

Where I_{os} = reverse saturation current, v = diode voltage, q = electronic charge, k = Boltzmann's constant, T = temperature.

The static power delivered is the multiple of supply voltage and leakage current. The static power dissipation is expressed as

$$P = nI \times V_{dd} \quad (2)$$

Where n = number of devices, V_{dd} = supply voltage, I = Leakage current

II. Conventional Full Subtractor

A full Subtractor is an accumulated circuit which performs subtraction of 2- bits out of which 1 has been borrowed by a lesser important stage. The Full Subtractor circuit has 3-inputs and 2-outputs. Out of which A, B and C are applied at the different gates and outputs are gated correspondingly. The three inputs contain three 1- bit binary numbers A, B and C. The gate level implementation of each Full Subtractor has been given. The output D is denoted for a difference bit and B is denoted for a borrow bit. The gates used to build the Subtractor have their own specifications and aren't distorted during this work, the gate level diagram of full Subtractor.

In subtracting a 2-bit number the subtrahend is mainly considered. The logical bit '1' is borrowed from the adjacent lower bit. Which results in the 3 bits to be engage in the input end of a Full Subtractor, predominantly a borrow bit designated as C and the two bits to be subtracted. The 2- outputs are mainly the Difference D and the Borrow Bout. Borrow output bit shows if the number bit has to borrow a '1' from the next probable higher number bit.

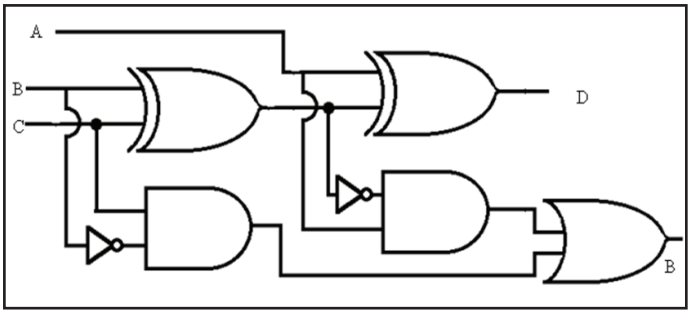

Fig. 1: Logic gate Design of Full Subtractor

The simple Boolean functions of output can be acquired from the truth table. The logic equations are

$$D\ (Difference) = A \oplus B \oplus C \quad (3)$$

$$\mathrm{B}\ (Borrow) = A'B + A'C + BC \quad (4)$$

Truth Table describing Full Subtractor nature is given in Table 1.

Table 1: Truth Table of Conventional Full Subtractor

A	B	C	Bout	Diff
0	0	0	0	0
0	0	1	1	1
0	1	0	0	1
0	1	1	0	0
1	0	0	1	1
1	0	1	1	0
1	1	0	0	0
1	1	1	1	1

III. Self Controllable Voltage Level (SVL) Full Subtractor

The contemporary VLSI technology prerequisite for devices working at Low-Power and provide high performance. The design necessities of contemporary technology can get hold of by SVL technology. A Self Controlled voltage level technique can be used as control circuit, either at the upper end of the unit in order to reduce the value of supply voltage termed as U-SVL technique or to lift the potential of the ground node at the lower end of the unit, termed as L-SVL technique. By means of this technique reduction in the power dissipation is achieved. The power dissipation is highly lessened when compared to the conventional design. The entire effect of this technique on the power consumption is illustrated fig. 2.

A. Full Subtractor via U-SVL technique

The U-SVL technique is a combination of a PMOS and two NMOS transistors that are linked in parallel. Here an input clock pulse is driven to the PMOS of U-SVL circuit and the remaining all NMOS are connected to drain terminal. Full Subtractor using U-SVL design is shown in fig. 2. Under this format, full supply voltage V_{dd} is driven to the semiconductor device. The U-SVL representation is anticipated on a wide channel pull up p-MOSFET and pull down n-MOSFET.

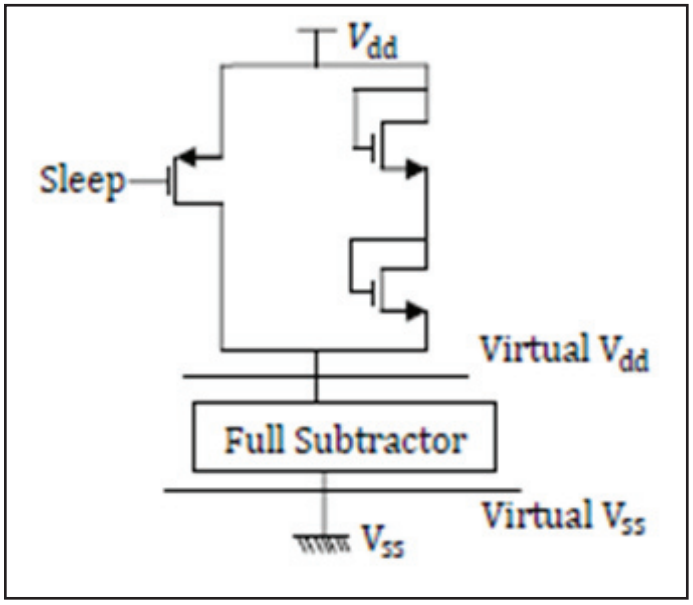

Fig. 2: U-SVL Scheme of Full Subtractor

The circuit of a full Subtractor is intended by U-SVL technique. This approach is not only important for sinking the power consumption but also for the leakage current. For small Power consumption applications, U-SVL technique is most accountable. Subtractor premeditated at micron CMOS technology, produces the healthier results. But in present scenario of nanotechnology at V_{dd} = 0.7V, Power consumption is 1.622μw.

III(b). Full Subtractor via L-SVL Technique

The L-SVL system is an incarnation of an NMOS and two PMOS are linked in parallel. Consequently an input clock pulse is applied at the NMOS of L-SVL circuit and the remaining all PMOS are connected to the ground. The ground terminal is allied to the L-SVL circuit. Full Subtractor using L-SVL scheme is given in fig. 3. The switch bears 0 Volts at the ground node and heaves the ground level (virtual ground). The L-SVL circuit commences a wide channel pull down n-MOSFET and pull up p-MOSFET.

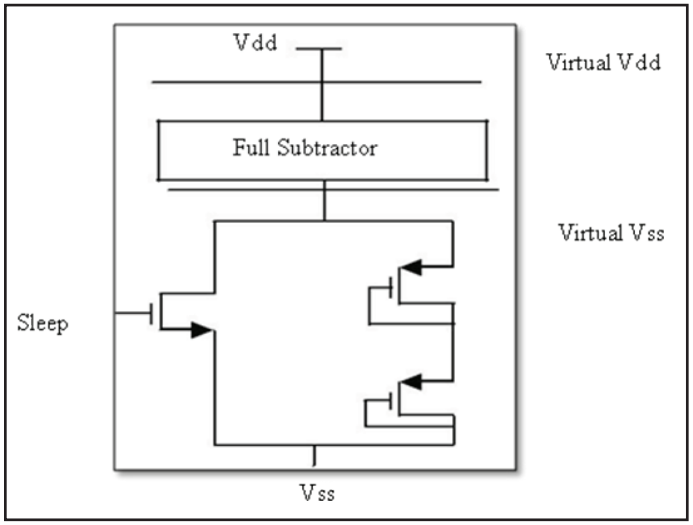

Fig. 3: L-SVL Scheme of Full Subtractor

Based on the inputs and the clock, deviation in output is assorted. Fig. 3 shows the difference of power supply voltage Vs of Full Subtractor devise with L-SVL system. Where the power consumption is calculated at a different supply voltage of V_{dd} = 0.7 V, power consumption is 1.24μw.

III(c). Full Subtractor via SVL Technique

The SVL devise encompasses an upper U-SVL circuit and lower L-SVL circuits, the diagrams shown in fig. 4 are implemented on the Full Subtractor. The U-SVL design makes use of a wide channel pull up p-MOSFET and a pull down n-MOSFET, so U-SVL and L-SVL design can offer higher supply voltage $V_d = V_{dd}$ and a abridged ground-level voltage V_s ($V_{ss} = 0$).

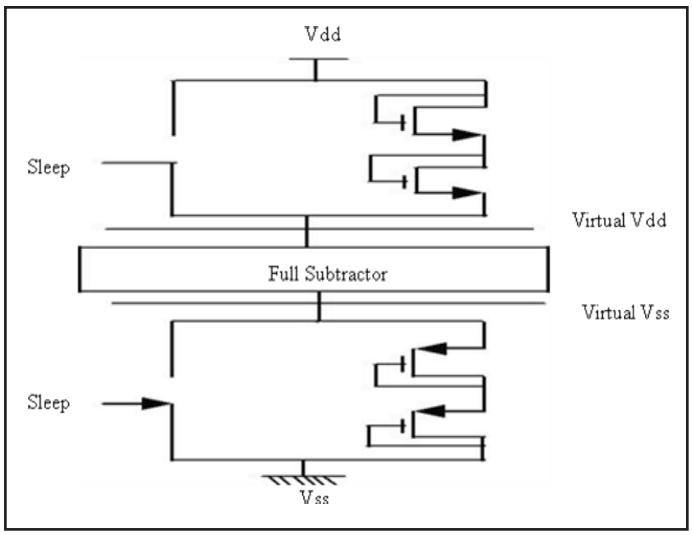

Fig. 4: SVL Technique of Full Subtractor

The U-SVL and L-SVL circuit equally engender an inferior supply voltage $V_{dd} = V_{dd}$ Vn < Vdd and a relatively superior ground-level voltage $V_s = V_p > 0$V, where V_n and V_p are the total voltage go down to all U-SVL and all L-SVL, correspondingly.

D. Layout Diagram Full Subtractor with SVL Technique

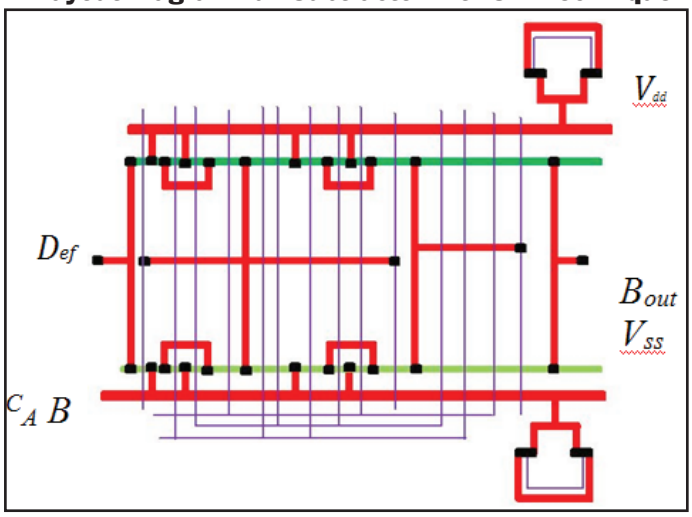

Fig. 5: Layout of Full Subtractor using SVL Technique

The Layout of Full Subtractor through self controllable voltage level (SVL) Technique is shown in fig. 5, in which an extra circuitry for controlling the leakage current is used. SVL is classified into two blocks- namely upper SVL (U-SVL) and lower SVL (L-SVL).U-SVL is connected to Vdd and L-SVL is connected to ground. In both upper and lower SVL comprises of 1- NMOS and 1- PMOS and gates are connected and applied a pre-charge voltage of 1V.

IV. Simulation Results

The circuit work simulated in intonation for 45nm technology, from the consequence table, an effective and standard reduction results in delay, leakage power and Leakage Current with SVL method contrast to U-SVL and L-SVL technique

A. Leakage Power

In Full Subtractor, due to the early switching of opposite level leakage the transistors are either in off mode or in ON mode. The power utilization in Full Subtractor munch through a power off 1.66nW, with U-SVL and through L-SVL procedure power munch through is 2.16nW therefore the typical outcome of Full Subtractor with SVL (both U-SVL and L-SVL) method 0.45pW, power reduction is achieved. This illustrates extra power drop in contrast to U-SVL and L-SVL at 45nm technology, so from this we examine a power drop of 24% using SVL practice with Full Subtractor. It can also be experimental all the way through varied supply voltage as shown in Table 2.

$$P_{leakage} = I_{leakage} \times V_{dd} \quad (5)$$

Where, $P_{leakage}$ (Leakage Power) = $I_{leakage}$ (Leakage Current) × V_{dd} (power supply).

The leakage power is calculated by this modus operandi and we calculate the efficient power in Full Subtractor with SVL method with supply voltage $V_{dd} = 0.7$V

Table 2: Leakage Power

Voltage	$P_{leakage}$ of Full Subtractor	$P_{leakage}$ with U-SVL Tech	$P_{leakage}$ With L-SVL Tech	$P_{leakage}$ with SVL Tech
0.6V	0.58	0.56	0.58	0.54
0.7V	2.16	2.11	1.79	1.89
0.8V	5.54	5.69	4.45	4.57
0.9V	10.38	10.20	8.53	8.55
1.0V	17.51	17.37	12.49	12.50

Simulation consequences have been shown in fig. 6 and it is apparent that Leakage power is boosted with the power supply. Figure also depict that the power dissipation is less as weigh against to LEVEL-4 at 0.6V to 1.0v input supply.

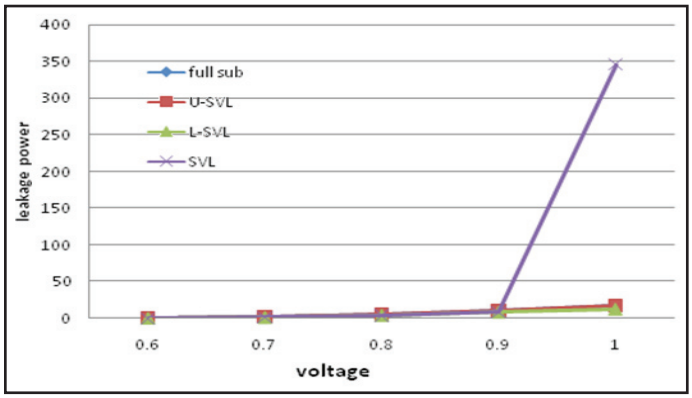

Fig. 6: Leakage Power Analysis

B. Leakage Current

The transistors are either in off mode or in ON mode in a Full Subtractor, due to the early switching of contradictory level leakage. The Leakage Current in Full Subtractor, a Current of 6.21mA, with U-SVL and with L-SVL technique Leakage Current is 4.21mA then, hence we finally get the average result of Full Subtractor with SVL (both U-SVL and L-SVL) technique, this shows additional Leakage reduction in contrast to U-SVL and

L-SVL at 45nm technology, so from this we analyze a Power drop of 24% using SVL technique by means of Full Subtractor. Power dissipation in any Full Subtractor circuit depends on both static and dynamic power indulgence. The static power delivered is the multiple of supply voltage and leakage current. The leakage current is described by the equation (1).

Table 3: Leakage Current

Voltage	$P_{leakage}$ of Full Subtractor	$P_{leakage}$ With U-SVL Tech	$P_{leakage}$ With L-SVL Tech	$P_{leakage}$ With SVL Tech
0.6V	2.16	1.72	3.57	125.0
0.7V	5.89	2.33	169.08	180.5
0.8V	9.24	8.84	227.4	234.6
0.9V	12.59	51.26	285.5	296.2
1.0V	17.59	106.18	343.3	345.3

Simulation results have been shown in fig. 7 and it is clear that Leakage Current increases with the power supply. Fig. 7 also shows that the Leakage Current is less at compared to Level-4 at 0.6V to 1.0v input supply.

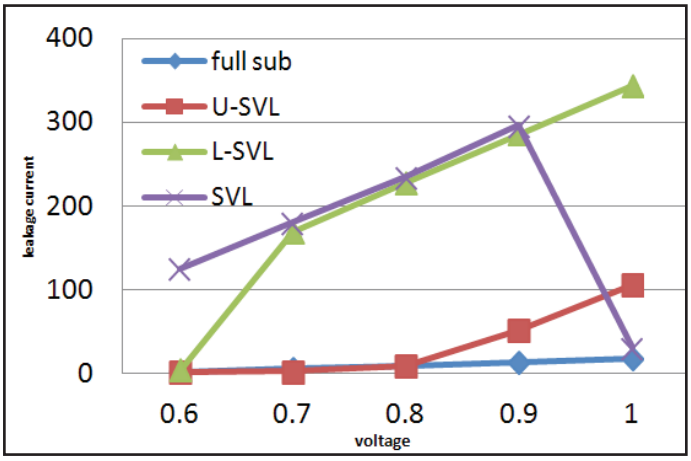

Fig. 7: Leakage Current Analysis

C. Delay

The time divergence among the input rising the reference voltage and output altering the logic state is recognized as the propagation delay. Propagation delay time of Full Subtractor input a superior input will effect in a slighter delay time.

Table 4 Delay Analysis

Voltage	Delay of Full Subtractor	Delay with U–SVL Tech	Delay with L–SVL Tech.	Leakage Power with SVL Tech. (both U-SVL and L-SVL)
0.6V	4.20	3.20	1.22	3.52
0.7V	9.33	5.38	3.24	6.26
0.8V	15.64	7.23	6.05	10.70
0.9V	21.32	10.22	8.30	18.65
1.0V	27.00	15.62	12.04	30.42

Delay time of the circuit is deliberate as the average of response time of gate for positive. The proportional analysis of different circuit delay time is shown in Table 4.

Simulation results have been uncovered in Figure 8 and it is apparent that Delay augments with the power supply. Figure 8 also shows that the Delay is less at compared to Level-4 at 0.6V to 1.0v input supply.

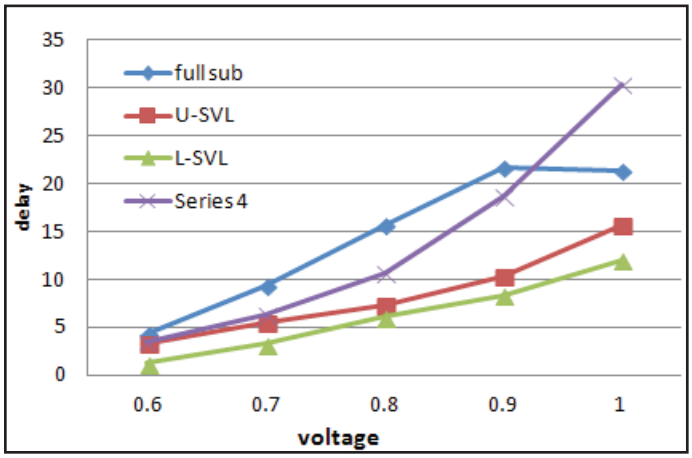

Fig. 8: Delay Analysis

V. Conclusion

The Simulation results undoubtedly explain the decrease in the power utilization by included with SVL technique that is either U-SVL or L-SVL technique. Anticipated Full Subtractor is tailored by using transistors having fewer average power consumption with decreases in delay is also lessen by using only PMOS as because delay is more concerted to PMOS due to less Power, delay and Leakage Current, SVL based Full Subtractor is created by using transistor and have enhanced performance than the U-SVL and L-SVL Full Subtractor as there are smaller number of transistor counts by which area is reduced and delay is also reduced; the average power expenditure of the proposed Full Subtractor is less in association to the conventional Full Subtractor, calculated result appropriately verified the principle of operation and characteristic of the low-power Full Subtractor circuit. The circuit has been used for propose of low power. On conniving SVL technique based full-Subtractor with 45 nm technologies, we attain a very stumpy power consumption circuit, a reduced amount of propagation delay and also with lesser number.

References

[1] B. Dilli Kumar, M. Bharathi,"Design and Analysis of Adaiabatic Full Subtractor for Low Power Applications", International Journal of Advanced Scientific and Technical Research, Vol. 1, No. 3, pp. 219-231.

[2] D. A. Antoniadis, I. Aberg, C. N. Chleirigh, O. M. Nayfeh, A. Khakifirooz, J. L. Hoyt,"Continuous MOSFET performance increase with device scaling: The role of strain and channel material innovations", IBM Journal Research Development, Vol. 50, No. 4, pp. 363–376, Jul. 2006.

[3] K. Roy, S. Mukhopadhyay, H. Mahamoodi-Meimand, "Leakage current mechanisms and leakage reduction techniques in deep sub-micrometer CMOS circuits", In Proceeding IEEE, Vol. 91, No. 2, pp. 305– 327,Feb. 2003.

[4] S. Dutta, S. Nag, K. Roy,"ASAP: A Transistor Sizing tool for speed, area, and power optimization of static CMOS circuits", IEEE International Symposium on Circuits and Systems, Vol. 1 pp. 61-64, June.1994.

[5] B. Dilli Kumar, M. Bharathi,"Design and Analysis of Adiabatic Full Subtractor for Low Power Applications",

International Journal of Advanced Scientific and Technical Research, Vol. 1, No. 3, pp. 219-231.
[6] P. Sharma, Anjali Sharma, Richa Singh,"Design and analysis of area and power efficient 1-bit Full Subtractor using 120nm technology", International Journal of computer application, Vol. 88, No. 12, pp. 1-42, Feb. 2014.
[7] Tanvi Sood, Rajesh Mehra,"Design a Low Power Half-Subtractor Using .90μm CMOS Technology", IOSR Journal of VLSI and Signal Processing, Vol. 2, No. 3, pp. 57-61, Jun 2013.
[8] Mutoh S,"1-V Power supply high-speed digital circuit technology with multi-threshold voltage CMOS", IEEE J. Solid State Circuits, Vol. 30, pp. 847-854, August 1995.
[9] Hemantha S, Dhawan A, Kar H,"Multi-threshold CMOS design for low power digital circuits", TENCON 2008-2008 IEEE Region 10 Conference, pp. 1-5, 2008.
[10] H. Thapliyal, M.B Srinivas, H.R Arabnia,"Reversible Logic Synthesis of Half, Full and Parallel Subtractors", Proceeding of the 2005 International Conference on Embedded Systems and Applications, Las Vegas, pp. 165-181.
[11] Phanikumar M, N. Shanmukha Rao,"A Low Power and High Speed Design for VLSI Logic Circuits Using Mult-Threshold Voltage CMOS Technology", International Journal of Computer Science and Information Technologies (IJCSIT), Vol. 3(3), pp. 4131-4133, 2012.
[12] H. Thapliyal, N. Ranganathan,"Conservative QCA Gate (CQCA) for Designing Concurrently Testable Molecular QCA Circuit", Proceeding of the 22nd International Conference on VLSI Design, New Delhi, India, pp. 511-516, 2009.
[13] Majid Mohammadi, Mohammad Eshghi, Majid Haghparast, Abbas Bahrololoom,"Design and Optimization of Reversible BCDAdder/Subtractor Circuit for Quantum and Nanotechnology Based Systems", World Applied Sciences Journal, Vol. 4, No. 6, pp. 787-792, 2008.
[14] Zimmermann R., Fichtner W.,"Low-power logic styles: CMOS versus pass-transistor logic", IEEE Journal Solid-State Circuits, Vol. 32, No. 7, pp. 1079-1090, 1997.
[15] J. Kao, A. Chandrakasan, D. Antoniadis,"Transistor sizing issues and tool for multi-threshold CMOS technology", In proceeding 34th DAC, pp. 409-414, 1997.
[16] Monpapassorn,"Programmable wide range voltage adder/ Subtractor and its applications an encoder", IEEE Proceeding of Circuits Devices and Systems, Vol. 152, pp. 697-702, 2005.
[17] R. Fried, C. C. Enz,"Simple and accurate voltage adder/ Subtractor", Electronics Letters, Vol. 33, pp. 944-945.
[18] Andrew Bailey, Ahmad AlZahrani, Guoyuan Fu, Jia Di, Scott Smith,"Multi-threshold Synchronous Circuit Design for Ultra-Low Power", Journal of Low power Electronics, Vol. 4, pp. 1-12, 2008.

Bikshalu Kalagadda was born in 1980. He received his B.Tech, M.Tech and Ph.D from Jawaharlal Nehru Technological University Hyderabad in 2002, 2007 and 2015 respectively. Currently he is working as an Assistant professor in the Department of Electronics and Communication Engineering, Kakatiya University Warangal. His current research interests include Nano electronics and nano devices for future technologies.

Madhavi Latha Pedada was born in 1991. She received his B. Tech degree from JNTU Kakinada in 2012. She is currently pursuing M.Tech degree from Kakatiya University Warangal. Her current research interests include Nano electronics and nano devices for future technologies.

Keerti Kumar Korlapati was born in 1985. He received his B. Tech degree from JNTU Hyderabad in 2006. He received his Master of Engineering degree from Osmania University in 2008. Currently he is working towards his Ph.D degree from National Institute of Technology Warangal. His current research interests include Device Modeling, Nano scale semiconductor devices, Nano biomedical electronic sensors and MEMS.